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SPECIAL APPLICATIONS OF THE DM7800 VOLTAGE TRANSLATOR

INTRODUCTION

The DM7800/8800 is a dual voltage translator designed to provide interfacing between standard bipolar TTL or DTL logic levels and MOS logic levels. The basic circuit description, parameter guarantees, and theory of operation are covered on the data sheet. This technical note will describe the circuit characteristics in more detail, to show trade-offs which can be made to allow a wider range of operating conditions than is implied on the data sheet.

There are only three types of terminals on the device whose conditions could possibly be varied. These are the inputs, outputs, and the power supplies.

INPUTS

Little needs to be said about the conventional diode inputs. They buffer the circuit and help to establish the threshold of the translator. Together with the input resistor, R1 (see Figure 1), they limit the logical "0" input current to 0.4 mA (max) thus reducing the "OFF" level power dissipation.

OUTPUT AND VARIABLE POWER SUPPLIES

Separation of these two areas of the circuit is impossible due to the interaction they have with one another. The data sheet guarantees that V_2 may vary from -8V to -25V and V_3 can extend to +25V, so long as under normal operating conditions there is never more than a 33V differential between V_2 and V_3. Over this range of conditions the output voltage swing is from V_3 to $V_2 + 2V$ as the device is switched.

LOWER OUTPUT IMPEDANCE

In addition it is guaranteed that the output resistor, R5, will be between 12K and 20K. Within this range of operation there are various things which can be done to the output to tailor its characteristics for a particular job. For example, although the nominally 16K output resistor was chosen to minimize power dissipation for analog switching applications, it is desirable in some applications to lower this value, to increase the speed of response. This can be done without exceeding the device limitations, if full output voltage swing is not required.

The data sheet guarantees that with a differential of +33V between V_2 and V_3 and Q3 in the "ON" state, the output voltage will never be more positive than $V_2 + 2V$. This leaves at least 31 volts across the output resistor. So that typically the output is capable of sinking at least $\frac{33V - 2V}{16K} = 2.0$ mA. Worst case, however, there is no guarantee that Q3 is capable of sinking that much current. The reason is that the output resistor may have been 20K so that in testing, the device was tested under a load current of $I = \frac{33V - 2V}{20K} = 1.55$ mA. This means that any translator was tested under at least this much current load. Most devices will be able to function while sinking somewhat more than this; but the user can be guaranteed that at least this value will result in safe operation. If the actual output resistor value were measured more current drive could be anticipated.

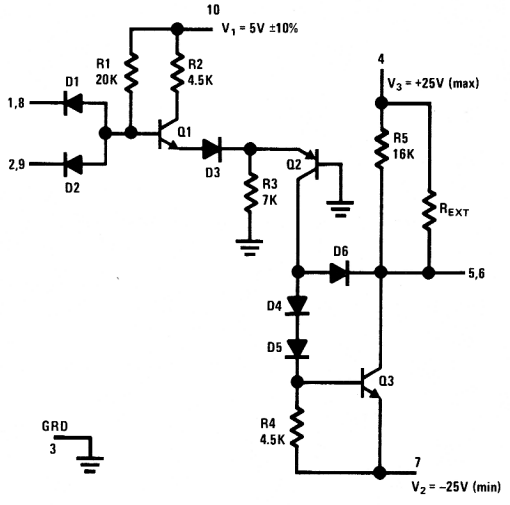

Figure 1. DM7800 Circuit Diagram

What is implied by looking at the output from a current standpoint is that the output resistor may be paralleled (Figure 1) to reduce the effective value so long as the resulting combination of resistance and voltage across that resistance does not produce in excess of 1.55 mA through the output transistor. Calculation of the value of this resistor is performed as follows:

$$1.55\ mA = I_{R_{INT}} + I_{R_{EXT}}$$

$$= \frac{V_3 - (V_2 + 2)}{20K} + \frac{V_3 - (V_2 + 2)}{R_{EXT}}$$

$$R_{EXT} = \frac{V_3 - (V_2 + 2)}{1.65 - .05\ (V_3 - V_2)}$$

Essentially, voltage swing is traded for lower output impedance, while still keeping the translator within its guaranteed operating range.

HIGHER DRIVE CAPABILITY

Some applications require a higher capacitive drive capability than the output can normally provide. Again at the sacrifice of voltage swing, this is possible.

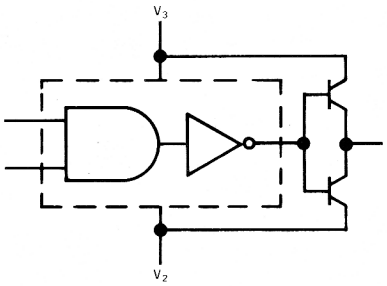

Figure 2. Output Buffering

This circuit can also be used to increase the DC drive capability of the device; however, under worst case conditions the output voltage of the DM7800/8800 will degrade 2V for every 0.1 mA of base current required by the NPN or PNP transistors due to additional current into the 16K resistor or Q3. Typically this would be 1.6V per 0.1 mA for the NPN transistor, but an insignificant amount of voltage for 0.1 mA of PNP base current. Also if the differential between V_2 and V_3 were reduced the output of the DM7800/8800 would have 0.1 mA of base drive available for the PNP, for every two volts reduction of $V_3 - V_2$.

SUPPLY VOLTAGE VARIATION

It is also possible under certain conditions to operate the translator with a V_2 slightly more positive than the data sheet limit of -8V. This limit was selected to insure that under worst case conditions there would be enough voltage to forward bias the base-emitter junction of Q3 and the diodes D5 and D6. At low temperature this would approach 3V. In addition the h_{FE} of Q2 is a strong function of the collector-base voltage. A -8V limit would still allow -5V collector-to-base on Q2; and therefore a reasonable h_{FE} could be obtained from a normally low h_{FE} type transistor (lateral construction). This allows the guaranteeing of a full differential of 33 volts from V_3 to V_2.

As before however, output voltage swing can be traded for another parameter – in this case, the V_2 voltage. Operation of the V_2 supply more positive than -8V is not within guaranteed operation, but as shown in Figure 3, by reducing the $V_3 - V_2$ differential voltage significantly, operation to -4.5V on V_2 is achievable, and reliable.

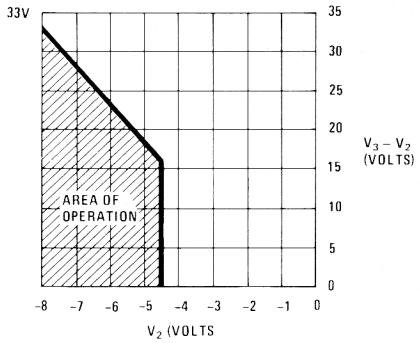

Figure 3. Extended Area of Operation

MEASUREMENT TECHNIQUES

The last item to be mentioned does not come under the category of changing the device's characteristics, but rather with how to measure the characteristics. When dealing with a high output impedance device such as that of the DM7800 and attempting to make measurements of switching times, the measurement techniques are very important. Quite often the device appears to be slower than it actually is, due to test board and measuring equipment capacitances. For example a 10 pF scope probe would add about 320 ns to the rise time of a typical unit (10% to 90%). This increase due to evaluation procedures may be equivalent to, or even greater in magnitude than the normal rise time of the unit in the circuit. Thus the results obtained may be completely invalid. Care should therefore be taken in construction of test fixtures, and low capacitance probes used if any meaningful data is to be obtained.

CONCLUSION

The subjects discussed here were designed to show that if sound engineering principles are followed, trade-offs in some output parameters can be made to improve performance in others. These trade-offs are made possible by analyzing the true meaning of the guaranteed specifications and how they relate to the circuit. In addition care and caution were urged in regards to AC measurements, so that breadboard evaluations are meaningful, and so that the full potential of the unit can be realized and used.

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